2811

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13
10-20-00
C Brown

Application of

Applicants	:	Fernando Gonzalez and David Kao
Serial No.	:	09/375,081
Filed	:	August 16, 1999
Title	:	TRANSISTORS HAVING CONTROLLED CONDUCTIVE SPACERS, USES OF SUCH TRANSISTORS AND METHODS OF MAKING SUCH TRANSISTORS
Docket	:	MIO 0007 NA
Examiner	:	G. Munson
Art Unit	:	2811

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on October 11, 2000.

Gregory J. Adams Reg. No. 44,494

Sir:

REPLY BRIEF UNDER 37 CFR 1.193(b)

Reply Brief noted
26 Oct 2000

This Reply Brief is filed in response to the Examiner's Answer mailed August 25, 2000. The Examiner's Answer raised a number of points in responding to the arguments presented in the Brief On Appeal filed on May 15, 2000. This Reply Brief is directed to addressing these points.

Remarks

The Examiner states that Rao '139 (U.S. Patent No. 4,213,139) (figure 3) discloses a transistor with two gates 15 and 16 and that Rao '263 (U.S. Patent No. 4,319,263) (figure 3) also discloses a transistor with two gates and in Figure 8 discloses a transistor with three gates 15, 16 and 41. The Examiner asserts that the two gate transistor may be represented by an equivalent circuit of two transistors as in figure 2, and the three gate transistor may be represented by an equivalent circuit of the three transistors as in figure 7. However, Applicants submit that a two transistor circuit fails to anticipate a single transistor with two gates and that a three transistor circuit fails to anticipate a single transistor with three gates.

Further, Applicants submit that neither Rao '139 nor Rao '263 disclose a multigate transistor.

The Examiner also states that the "spacer" does not distinguish over Rao '139 nor Rao '263. Applicants maintain that the spacer of Applicants' claims is not taught by Rao '139 nor Rao '263. Applicants' spacer is formed on the secondary oxide layer which is formed over the gate structure as recited in the appealed claims, whereas Rao '139 and Rao '263 only teach partly overlapping a gate with another gate from a second transistor. Additionally, at least a portion of Applicants' spacer is conductive. Applicants' spacer has both conductive portions and non-conductive portions.

Additionally, Rao '139 and Rao '263 fail to teach "a first contact to said gate structure" and "at least a second contact to said conductive portion of spacer" as recited in claim 15.

Conclusion

For the reasons set forth herein and in the Brief On Appeal filed on May 15, 2000, the Board of Patent Appeals and Interferences is respectfully requested to reverse the decision of the Examiner in rejecting claims 15-19 and 23 of the present application.

Respectfully submitted,

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